CHAPTER MEETINGS

SCV-CE - 8/31 | **New Developments in HDMI** - improvements, issues, 3D, interface, developments (new date) ... [more]

SCV-CAS - 9/1 | **Ultra-Low-Voltage VLSI Design for Minimum Energy Computing** - subthreshold CMOS, tradeoffs ... [more]

SCV-TMC - 9/2 | **Technology Management and Green Entrepreneurship** - Thinking outside the glass box, the power of green ... [more]

SCV-Phot - 9/7 | **Medical Image Processing in Ophthalmology and Beyond** - processing methods, state of the art, support clinicians... [more]

SCV-ComSoc - 9/8 | **High-Speed Transmission on Twisted Pair in LANs and DSL** - 2 talks: 1-GBASE-T, EEE, vectored DSL ... [more]

SFBAC - 9/8 | **The Smart Grid: From Appliance to Generator and Back** - 1-day webinar: control, security, applications, services ... [more]

SCV-CS - 9/14 | **Multicore Programming: Pitfalls and Solutions** - race conditions, finding, reproducing, debugging ... [more]

SCV-CNSV - 9/14 | **How to Be an Effective Technical Consultant by Speaking the Language of Business** - point of view, feedback... [more]

SCV-EDS - 9/14 | **LDMOS: Technology and Applications** - lateral diffusion, dc-dc converters, layout techniques ... [more]

SCV-EMB - 9/15 | **The Art of Catheter-Based Imaging** - interventional cardiology, diseases, ultrasound, optical ... [more]

SCV-PELS - 9/15 | **From Carbon-based to Sustainable Energy: What We Can Learn from "How Big Things Happen" in America** [more]

OEB-IAS - 9/16 | **PV Solar Plants – Controls and Inverters** - utility-scale plants, expectations ... [more]

SCV-CSS - 9/16 | **Patent Strategies for Entrepreneurs and Innovative Thinkers** - general principles, tools, working examples ... [more]

SCV-CAS - 9/20 | **Silicon Photonics: Opportunities & Challenges** - low cost, sensing, analysis, recent results ... [more]

SCV-Nano - 9/21 | **SolFocus Concentrator Photovoltaics** – An Introduction - what it is, how it works, where to use ... [more]

SCV-Mag - 9/21 | **Thermally-Assisted Magnetic Recording at up to 1 Tb/in^2 using an Integrated Plasmonic Antenna** – technologies [more]

Continued on next page ====>

Local Chapter Seminars & Webinars

9/8: IEEE Webinar -**The Smart Grid: From Appliance to Generator and Back** - a full-day webinar [more]

9/23-24: **EMC Modeling and Design; Radiated Immunity and Cosite Interference** - Doubletree Hotel [more]

9/25 | **Smart Grid Workshop: M2M Communications, Emerging Devices and "The Internet of Things"** - six talks in two tracks ... - SCU, 1:00 PM [more]

Conference Calendar

Sept 16: **GSA Emerging Opportunities Expo & Conference** - Santa Clara Convention Center [more]

Oct 3-8: **32nd Annual EOS/ESD Symposium & Exhibits** - Nugget Resort, Reno, NV [more]

Oct 12: **Cloud Forum for Practitioners: The Cloud in 2013** - Naval Postgraduate School, Monterey [more]

Oct 18-20: **Smart Grid Electronics Forum (SGEF)** - Crowne Plaza Hotel, San Jose [more]

Nov 9-11: **AdvancedTCA/MicroTCA Summit** - Santa Clara Convention Center [more]

Nov 14-18: **36th Int'l Symposium for Testing and Failure Analysis** - InterContinental Hotel, Dallas [more]

Dec 8-10: **3D Architectures for Semiconductor Integration and Packaging** - Hyatt, Burlingame [more]

CALL FOR PAPERS:
International Symposium on Quality Electronic Design - March 14-16, 2011 - Due **Sept. 30th** [more]

Career Development

Professional Skills Courses [more]
- 5 Habits of Intentional Leadership - Virtual Teams: Working Together Apart - Management Essentials - *and more*

Classes for Working Engineers [more]
- Python - C++ - Java - Embedded Linux - IC Design – Cryptography - Digital Signal Processing *and more*

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CHAPTER MEETINGS

(continued from Page 1)

SCV-CPMT - 9/23 | **Design of High Density & 3D Packaging: Tools and Knowledge** - electrical, thermal, manufacturing ... [more]

SCV-ComSoc - 9/25 | **Smart Grid Workshop: M2M Communications, Emerging Devices and "The Internet of Things"** ... [more]

SF-IAS - 9/28 | **Short Circuit, Device Coordination, and Arc Flash Analysis** - trends, new concepts, exposure, calculations ... [more]

SCV-PSES - 9/28 | **What's in Your Electronic Product, and Why Should a Product Safety Engineer be Concerned?** ... [more]

SCV-Rel - 9/29 | **Development and Application of Accelerated Test Methods Specific to CPV Systems** - results, lifetime [more]

OEB-Life - 10/5 | **Kickoff Meeting - IEEE Life Members Affinity Group** - activities, speakers, location of meetings ... [more]

SCV-TMC - 10/7 | **Building Powerful Relationships** - interpret behaviors, better understanding, de-escalate conflict ... [more]

SCV-CS - 10/12 | **High Performance Computing: Union of Software and Reconfigurable Logic** - FPGAs, app'ns ... [more]

SCV-CPMT - 10/12 | **All-Silicon System with Nano-Packaging: Highest Functionality, Lowest Cost, Smallest Size** ... [more]

SCV-EDS - 10/12 | **Is It the End of the Road for Silicon in Power Management?** - power MOSFETs, , bounds, GaN ... [more]

SCV-ComSoc - 10/13 | **40/100 Gigabit Ethernet: Market Needs, Applications, and Standards** - aggregation, , architecture ... [more]

SCV-CAS - 10/18 | **Automated Behavioral Modeling: A Quantum Jump in Mixed-Signal Design Verification Technologies** .. [more]

SCV-SSC+SPS+CAS+ComSoc - 10/21 | **Tutorial: Status of Knowledge on Non-Binary LDPC Decoders** – decoding ... [more]

SCV-Rel - 10/27 | HCPV **Tracker Accelerated Reliability Tests** - failure modes, time-to-failure distribution, wear-out modes ... [more]

SCV-CPMT - 10/28 | **Good Things Come in Small Packages** - portable connectivity, performance, low cost, growth trends ... [more]

SCV-CPMT - 11/10 | **Embedded Passives: Packaging Paradigm of the Future?** - benefits, when to implement, examples ... [more]

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

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IEEE Professional Skills Courses

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Managing Time & Multiple Priorities

- Date/Time: Wednesday, Sept 9, 9:00AM-1:00PM
- Instructor: Peter Turla
- Location: Integrated Device Technology, San Jose
- Fee: $300 for IEEE Members; $350 non-members

This is the best class I have ever taken. Brilliant! Thoroughly enjoyed it and will recommend to all my colleagues.
eBay, Inc. Attendee

Preparing Presentations to Decision Makers

- Date/Time: Thursday, Sept. 16, 9 AM – 5 PM
- Location: – TIBCO Software, Palo Alto
  Fee: $400 for IEEE Members; $500- non-members

This was all invaluable, I feel someone was talking who really knew the subject from the inside
-Philips Semiconductor

Management Essentials

- Date/Time: Thurs-Fri, Oct 7-8, 9 AM – 5 PM
- Location: – TIBCO Software, Palo Alto
  Fee: $625 for IEEE Members; $700 non-members

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Virtual Teams: Working Together Apart

- Date/Time: Thurs, Oct 12, 8:30AM – 4:30PM
- Location: – Trimble Navigation, Palo Alto
  Fee: $400 for IEEE Members; $500 non-members

5 Habits of Intentional Leadership

- Thur-Fri, Oct 14-15, 8:00AM-5:00PM
- Location: TIBCO Software, Palo Alto
  Fee: $625 for IEEE Members; $700 non-members

Identify leadership strengths, find opportunities to take risks needed for growth; build collaboration, teamwork and trust; strengthen the ability in others to outperform.

Collaborative Negotiating

- Date/Time: Wednesday Oct 27, 8:30 AM - 4:30 PM
- Instructor: Barry Flicker
- Location: EMC Software, Pleasanton
- Fee: $400 for IEEE Members; $450 non-members

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9:00 AM – 6:00 PM

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Day Two: Friday, September 24

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- **Radiated Immunity**
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NOTES:
The registration fee includes one copy of the technical program, continental breakfast, lunch, refreshment breaks each day, and the reception at the conclusion of the first day.

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There will be an exhibition on Thursday by vendors of EMC design, test and measurement related products and services. During the reception in the exhibit area, heavy appetizers and a no-host bar will be available. You are welcome to attend the reception only at **NO CHARGE**, provided a registration form is submitted in advance. Thus, if you can't join us for the entire day, drop by for the reception and exhibition to network with the speakers and attendees. You might even win a raffle prize!

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2. Electronic Design
- 2.1 System-level Design, Methodologies & Tools (SDM)
- 2.2 Package - Design Interactions & Co-Design (PDI)
- 2.3 Robust & Power-conscious Circuits & Systems (PCC)
- 2.4 Emerging/Innovative Process & Device Technologies and Design Issues (EDT)
- 2.5 Design of Reliable Circuits and Systems (DFR)
- 2.6 Design of Embedded Systems (ESYD)

3. Design Automation and CAD
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EDFAS GENERAL MEMBERSHIP MEETING

Wednesday, November 17

The Electronic Device Failure Analysis Society (EDFAS) annual General Membership Meeting and Luncheon is open to all current and interested prospective members.

ISTFA/2010 EDFAS Electronic Device Failure Analysis Society

One-Day Webinar - The Smart Grid: From Appliance to Generator and Back

Oregon Section, IEEE, in cooperation with the SF Bay Area Council

September 8, 2010

on the Internet

Time: 8:00 AM – 5:00 PM (PDT)

Location: at your Desktop PC

Cost: $99 for IEEE members; $150 for non-members, $25 for full-time students

Join us in this one-day workshop which provides a systems view of how the Smart Grid provides interactions between the end uses of electricity ("appliances" or industrial processes) and utilities, viewed from the perspective of the technologies, standards, and policies that will enable those interactions and foster innovation and interoperability.

The Smart Grid marries the electrical grid – an extremely complex system based on mature, conservative technology – with two fast moving innovative technologies: computers and communications. It is one of the greatest (if not *the* greatest) electrical, electronic and information processing challenges of our time and represents a significant engineering opportunity over the next two decades and beyond. It captures information about supply, system demand, individual usage, and pricing that fundamentally shifts how electricity is used. It enables the operators of the power system to increase efficiency and reliability while reducing costs and empowering consumers of electricity to minimize their own electricity costs.

Learning Objectives:

Attendees will gain an understanding of the monitoring, communications, security and control systems of the Smart Grid, how they interact, the flow of data and control, and design and implementation considerations including:

- Information requirements for optimal control of generating capacity, regional transmission grids, and municipal distribution grids to meet end user demands.
- How generation, transmission and distribution control systems utilize digital information.
- How suppliers and distributors of electricity use information to minimize costs while increasing reliability, flexibility, and security.
- How usage monitoring and automation will allow end users to make informed decisions that reduce their electricity costs.
- How to ensure grid security.
- Balancing optimization of the grid's subsystems and the grid as a whole.

Schedule

7:30 Web login and checking
8:00 Opening Remarks: Welcome, day plan
8:05 Opening Keynote: The Smart Grid – What will it take to make it possible; Saifur Rahman, IEEE Distinguished Lecturer, Virginia Tech
9:00 Controllability: The Challenge of Synchrophasors and Wide Area Control; Dmitry Kosterev, BPA
9:45 – 10:15 Break
10:15 Communications: Smart Grid Communications: You want how much bandwidth? And that little latency?; Joe Andres, BPA
11:10 Supply and Demand: Managing Supply and Demand: Supply and demand control methods and control points; Rob Pratt, PNNL
12:00 Lunch Keynote: Turning the Smart Grid Vision into Reality: A Policy Perspective; Jeff Hammarlund, Portland State University
1:10 Security: Smart Grid Cyber Security: Protecting the grid and its customers; Dave McKinnon, PNNL
2:10 Applications and Services: Smart Grid Enabled Applications and Services: What's the killer app (and for whom); Linda Rankin, Portland State Univ.
3:00 – 3:30 Break
3:30 Interoperability and Standards: What standards are needed/being developed to make the Smart Grid work; Steve Widergren, PNNL
4:30 – 5:00 Panel Discussion: Q+A with the speakers

Target Audience:

The target audience is engineers, policy makers, and entrepreneurs who want to understand the Smart Grid in order to make better professional, technical and business decisions.

Prerequisites:

Attendees should be generally familiar with the electric power system, software, or data communications concepts; a power engineering background is not required.

Download full information, including talk summaries, speaker biographies:

www.e-grid.net/docs/1009-smartgrid.pdf

Plan to attend!

(see next page ➔)

Smart Grid Electronics Forum

October 18-20 2010, San Jose, CA

Plugging Into The Smart Grid

Crowne Plaza Hotel, San Jose

– Sessions – Keynotes – Exhibits

Learn how deployment of the Smart Grid will change the design of all types of electronic equipment -- from the Smart Meter through the building to the end-use equipment. For design engineers in all segments of the electronics industry – Communications, Computing, Consumer, Power Conversion, Alternative Energy, Industrial, Medical.

TOPICS: - Real-Time control - power quality considerations - mission-critical customers - reliability and availability - distribution architectures - communications standards - smart appliances - networking/embedded processing - advanced metering - circuit design - instrumentation and monitoring - demand-side management - plug-in hybrid vehicles - Large-scale energy storage.

SGEF is for:

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- Technical editors and industry analysts

Register by **September 3**, to save.

Full details: **smartgrid.darnell.com**

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SCV Consumer Electronics

TUESDAY August 31, 2010

New Developments in HDMI

Speaker: Chandlee Harrell, Silicon Image
Time: Networking/refreshments at 6:30 PM; Presentation at 7:00 PM
Cost: $10 for non-members, $5 foe IEEE members, free for IEEE CES members & Student IEEE members
Place: Hewlett Packard, Building 20, 3000 Hanover St., Palo Alto
RSVP: from the website
Web: ewh.ieee.org/r6/scv/ce

HDMI (High-Definition Multimedia Interface) is that now-familiar interface that you use to connect video and audio to your HDTV set. It has gone through a number of improvements since it first came out, some of the latest issues having to deal with 3D. Come learn more about this interface and what is developing.

Chandlee Harrell

Sr. Director, System Architecture & Technology, Silicon Image, Inc.

Chief technologist for HDMI Licensing, LLC. Represent Silicon Image on the HDMI committee. Active Technical board member with respect to the new directions within HDMI including the exciting new features in HDMI1.4/HDMI1.4a.

Industry background in digital video, imaging, 3D graphics. Development of systems and components for digital TVs, streaming networks, video coding, and 3D graphics.

Tenures at Silicon Image, Silicon Graphics, Bell Labs, a startup or two.

Brown University, Stanford University

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SCV Circuits and Systems

WEDNESDAY September 1, 2010

Ultra-Low-Voltage VLSI Design for Minimum Energy Computing

Speaker: Massimo Alioto, Ph.D, Visiting Professor at BWRC -- UC-Berkeley
Time: Networking/light dinner at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation accepted for food
Place: QualComm Santa Clara, Building B, 3165 Kifer Road, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/cas

Massimo Alioto (M'01-SM'07) was born in Brescia, Italy, in 1972. He received the laurea degree in Electronics Engineering and the Ph.D. degree in Electrical Engineering from the University of Catania (Italy) in 1997 and 2001, respectively. In 2002, he joined the Dipartimento di Ingegneria dell'Informazione (DII) of the University of Siena as a Research Associate and in the same year as an Assistant Professor. In 2005 he was appointed Associate Professor of Electronics, and was engaged in the same faculty in 2006. In the summer of 2007, he was a Visiting Professor at EPFL - Lausanne (Switzerland). In 2009-2010, he is Visiting Professor at BWRC -- UCBerkeley, investigating on ultra-low power circuits and wireless sensor nodes.

Since 2001 he has been teaching undergraduate and graduate courses on advanced VLSI digital design, microelectronics and basic electronics. He has authored or coauthored more than 140 publications on journals (50+, mostly IEEE Transactions) and conference proceedings. Two of them are among the 25 most downloaded TVLSI papers in 2007 (respectively 10th and 13th). He is coauthor of the book Model and Design of Bipolar and MOS Current Mode Logic: CML, ECL and SCL Digital Circuits (Springer, 2005). His primary research interests include the modeling and the optimized design of CMOS high performance, low power and ultra low power digital circuits, arithmetic and cryptographic circuits, interconnect modeling, design/modeling for variabilitytolerant and low leakage VLSI circuits, circuit techniques for emerging technologies. He is the director of the Electronics Lab at University of Siena (site of Arezzo).

In the last years, subthreshold CMOS logic circuits have become very popular in ultra low power applications, which typically constrain the power budget to a few tens of uWs and the supply voltage to a few hundreds of mV. Designing at such low power and low voltage is challenging and requires a deep understanding of the power delay tradeoff, as well as of the impact of design variables and variability sources on the circuit robustness.

In this talk, a survey of fresh ideas and recent techniques to design and implement subthreshold CMOS logic circuits is presented. Novel circuit models of subthreshold CMOS logic in nanometer technologies are presented to understand its basic properties. The models are then used to derive design criteria to meet assigned constraints in the power delay design space, as well as to counteract with the issues that arise in nanometer technologies (process/voltage/temperature variations, leakage power, robustness...). Limitations under nanometer technologies are addressed in the scaling perspective. Design techniques are discussed at the physical, transistor, gate and system level of abstraction. Detailed guidelines on how to build ultra low power standard cell libraries are derived, and examples are provided. A detailed comparison of design flows targeting standard and subthreshold CMOS logic is also presented to understand how to specifically build design flows for ultra low power. Successful designs and state of the art chips are presented to gain a clear understanding of the state of the art, and which direction the research is moving to.

SCV Technology Management

THURSDAY September 2, 2010

Technology Management and Green Entrepreneurship: Thinking Outside the Glass Box

Speaker: Kevin Surace, Chairman & CEO, Serious Materials
Time: Networking at 6:00 PM; Forum at 6:30 PM; Dinner at 7:15 PM; Presentation at 7:45 PM
Cost: $10 for IEEE members; $13 for others
Place: RAMADA Silicon Valley, 1217 Wildwood Ave, Sunnyvale
RSVP: not required
Web: www.ieee-scv-tmc.org/

"Thinking Outside the Glass Box" - How an engineer built what Inc Magazine calls a "great company" by doing things differently, and recognizing the power of green.

Kevin Surace, a noted speaker and writer on climate change and the built environment, is on a mission to drive energy efficiency in the built environment, and bring green jobs and manufacturing back to the US. As CEO of Serious Materials, Kevin leads the company in its mission to reduce energy usage and CO_2 generation of the world's largest contributor, our buildings. Before joining Serious Materials in 2002, Mr. Surace held executive and technical positions with Perfect Commerce, General Magic, Air Communications, National Semiconductor, and Seiko-Epson. He received his degree in electrical engineering technology from Rochester Institute of Technology where he currently serves on the Board of Trustees, and has been awarded 9 patents. Mr. Surace also serves on the boards of Array Converter, Arch Rock, and Zeta Communities; and was recognized as 2009 Entrepreneur of the Year by Inc. Magazine

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Smart Grid Electronics Forum

Learn How the Smart Grid will Change the Design of Electronic Equipment

October 18-20, 2010

SCV Photonics

TUESDAY September 7, 2010

Medical Image Processing in Ophthalmology and Beyond

Speaker: Dr. Jonathan Oakley, Pixeleron
Time: Networking/Light Dinner at 6:00 PM; Presentation at 7:00 PM
Cost: none
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: ewh.ieee.org/r6/scv/leos

Dr. Jonathan Oakley studied Computer Science at the University of York, England. Following a Masters from the department of Medical Physics at University College, London, he completed his Ph.D. In medical image processing at the Swiss Federal Institute of Technology, Zurich. After academia he was relocated to San Jose while working for KLA-Tencor, but later returned to medical imaging with Fujifilm and then Carl Zeiss Meditec Inc. At Zeiss, Jonathan has worked exclusively on Optical Coherence Tomography images, leveraging his background in radiology to create and productize algorithms for the Cirrus™ instrument's motion correction, all Cirrus registration algorithms, Optic Disc centering (AutoCenter™), Corneal segmentation, Selective Pixel Profiling™, and the just-released Optic Nerve Head segmentation algorithm. More recently he has developed inner retina segmentation algorithms that have generated new scientific findings and consequently new market opportunities for ophthalmic imaging in the neurological domain.

In June of this year, Jonathan created an independent consulting firm, Pixeleron, specializing in medical image processing, and ophthalmology in particular. His talk will cover medical imaging processing methods, what is currently the state of the art, and how these are being used to support clinicians and radiologists. Particular emphasis will be given to ophthalmic applications.

This talk will cover medical imaging processing methods, what is currently the state of the art, and how these are being used to support clinicians and radiologists. Particular emphasis will be given to ophthalmic applications.

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Dr. Todd Hubing, Dr. Tom Jerse
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WEDNESDAY September 8, 2010

High-Speed Transmission on Twisted Pair in LANs and DSL

Speakers: Sanjay Kasturia and Jose Tellado, Teranetics; George Ginis, ASSIA, Inc
Time: Networking with refreshments at 6:00 PM; Presentations at 6:30 PM, followed by panel
Cost: none
Place: National Semiconductor, Building E, Conference Room, 2900 Semiconductor Dr, Santa Clara
RSVP: From the website
Web: www.ewh.ieee.org/r6/scv/comsoc

Sanjay Kasturia is the CTO and Chairman of Teranetics. Sanjay is also currently the editor-in-chief for the IEEE task force developing the Energy Efficient Ethernet standard and was previously the editor-in-chief for the 10GBASE-T standard. Before starting Teranetics, Sanjay co-founded Airgo Networks, now a part of Qualcomm, which developed wireless LAN ICs that significantly increased the range and reliability of networks using multi-antenna signal processing technology. Sanjay has previously served as Vice President Advanced Technology at Raychem's Telecommunications, Energy and Industrial Division, focusing on telecommunications and access network electronics. Before Raychem, Sanjay was at Lucent Technologies as R&D Director for its Global Wireless Products Group and earlier as head of Wireless Technology Research for Bell Laboratories. He holds a B.S. in Electrical Engineering from Indian Institute of Technology, Kanpur, and M.S. and Ph.D. in Electrical Engineering from Stanford University. Sanjay is a Fellow of the IEEE.

Jose Tellado is Vice President of Systems Engineering and co-founder of Teranetics. He is an expert in broadband communication systems specializing in high performance transceiver design and implementation. Jose was editor of the PCS section of the 10GBASE-T standard. Prior to Teranetics, Jose was the Modem Architect at Intel's Broadband Wireless Access group. As an employee-founder and Director of Technology at Iospan Wireless, Jose was the chief designer of the innovative MIMO-OFDM AirBurst™ technology at Iospan (acquired by Intel).

(continued, next page)

This session will address the challenges of high speed twisted pair-based communications in data centers/enterprises (LAN) and wireline access (DSL). There will be two talks followed by a panel session/ audience Q and A. The panel will be moderated by MP Divakar, ComSocSCV Program Operations Manager.

"**10GBASE-T and EEE: Advances in LAN Transport over Twisted Pair Media**",
Sanjay Kasturia and Jose Tellado of Teranetics

Structured twisted pair cabling has been the work horse of the LAN since it replaced coaxial cable in the mid-80s. A progression of standards, from 10BASE-T to 10GBASE-T has taken the Ethernet physical layer from simple Manchester signaling to a highly sophisticated communication link using THP, crosstalk cancellation and LDPC-based FEC. With each increase in speed, as the operating speed has inched closer to the capacity offered by twisted pair media, the industry has had to use more sophisticated tools from the communications theory toolbox to handle the reduced margin. As 10GBASE-T is moving from being "close to impossible" to widely available, with its complexity encapsulated in dual and quad port transceivers, there is now concern about its vulnerability to electromagnetic interference.

We first describe 10GBASE-T and its operation over twisted pair media. The interaction between external electromagnetic interference and the operation of 10GBASE-T links will be discussed. Techniques available for handling of electromagnetic interference will also be discussed. Next, we present an overview of Energy Efficient Ethernet (EEE), which is currently in the final stages of standardization in IEEE 802.3 standards committee. EEE borrows techniques widely used in wireless standards to reduce the average power consumption of Ethernet links.

"**Vectored DSL: How Crosstalk Cancellation Leads to 100 Mbps Broadband Access**", George Ginis of ASSIA, Inc

Vectored Digital Subscriber Line (DSL) technology pushes the data rates achievable over a single copper twisted-pair to the region of 100 Mbps. In addition, this is dedicated bandwidth for each customer, and not shared as in other broadband access systems using coaxial cable or Passive Optical Networks (PON).

(continued, next page)

Biographies (continued)

Earlier, while at Stanford University, Jose proposed new advanced methods for Multi-carrier Modulation (DMT/OFDM) in the areas of Peak to Average Power Ratio Reduction and Multi-user Transmit Optimization. Jose has also consulted for Apple Computer's Advanced Technology Wireless group and Globalstar in the areas of Wireless LAN and Low-Orbit Satellite cellular systems respectively. He is the author of 25 Patents, 15 IEEE publications and the book "Multi-carrier Modulation with Low PAR: Applications to DSL and Wireless" published by Kluwer. Jose holds MS. and Ph.D. degrees in Electrical Engineering from Stanford University.

George Ginis is currently Vice President of Expresse Engineering with ASSIA, Inc, overseeing development and deployment of the DSL Expresse management product, which enables service providers to maximise the performance of their DSL networks. He joined ASSIA, Inc in 2005, initially as Director of Technology, responsible for technology development, intellectual property and standards. Between 2002 and 2005, he was a systems engineer with the Broadband Communications Group of Texas Instruments, where he was involved in the design of DSL chipsets for central office equipment and residential gateways. He holds a diploma in electrical and computer engineering from the National Technical University of Athens, and MS and PhD degrees in electrical engineering from Stanford University. Dr Ginis is one of the key inventors of the Vectored DSL technology, defined in 2002 in his PhD thesis. He contributed heavily to industry efforts to develop the technology, which have led to the recent publication of the ITU-T recommendation G.993.5 (G.vector).

Talk Descriptions (continued)

Such speeds are achieved by reducing the crosstalk effects that limit data rate performance in dense deployment of DSL lines operating in the very-high-speed region. Major DSL chipset vendors have recently presented results from vectored DSL system prototypes and have introduced their first vectored DSL products, which realise the very substantial performance gains that were predicted by earlier theory.

An overview of the Vectored DSL technology will be presented. It will include an explanation of the principles of crosstalk cancellation, and a description of the techniques used for estimation of the crosstalk channel in DSL. Next, we'll explain initialization and "showtime" operation methods defined in the vectored DSL standard - ITU-T recommendation G.993.5. In the second part of the talk, we will cover the topic of management of Vectored DSL for maximizing performance. This will include descriptions of how to direct the systems' computational resources to realize the highest data rates, how to address the issue of time-varying noises, and how to deal with scenarios of mixed binders (co-existence of vectored and non-vectored lines).

SCV Electron Devices

TUESDAY September 14, 2010

LDMOS: Technology and Applications

Speaker: Shekar Mallikarjunaswamy, Alpha Omega Semiconductor
Time: Networking with pizza at 6:00 PM; Presentation at 6:15 PM
Cost: none
Place: National Semiconductor, Building E-1, Conference Center, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds

Dr. Shekar Mallikarjunaswamy received the B.Tech in electroncics (1987) and M.Tech in ICs and systems (1989) from the Indian Institute of Technology, Madras, India. He received the Ph.D in EE (1993) from NC State University, Raleigh, NC. He is currently Sr. Director at Alpha and Omega Semiconductor Ltd. Sunnyvale, responsible for PIC device technology, modeling, ESD and product design. He initiated development of TVS, analog and USB switch products at AOS, including development of proprietary 0.35um modular BCD technology. Prior to joining AOS, he worked in various managerial positions at Micrel, Impala Linear Corporation and Siliconix Inc. He has published over 30 technical papers in IEEE journals and conferences. He has won two best paper awards at IEEE conferences and holds over 25 US patents.

A key device that is used in most high voltage (20 to 120V) power integrated circuits for power management applications is the Lateral Diffused MOS (LDMOS) transistor. Recent interest in 'green" products have further increased the demand for integrated HV LDMOS devices in CMOS and BCD technologies to build higher efficiency dc-dc converters for consumer and LED markets. This presentation will journey through the structural innovations from "planar" to "trench" and to state-of-the-art "RESURF" LDMOS devices in both junction and dielectric isolation technologies for the past two decades. The physics of operation, figure of merits used for device comparison, layout techniques including integration of LDMOS into modern CMOS/BCD technologies will be discussed. Device and process simulations to optimize device parameters including SPICE macro circuits to model "quasi-saturation" and "Cgd" capacitance will be described. Methods to improve hot carrier reliability and ESD robustness of LDMOS devices will be highlighted. Finally, LDMOS circuit topologies and their applications in consumer, computer and telecommunication products will be presented to let the audience comprehend and appreciate the significance of LDMOS devices to modern power management products.

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TUESDAY September 14, 2010

How to Be an Effective Technical Consultant by Speaking the Language of Business

Speaker: John Levy, John Levy Consulting
Time: Networking and EnCorps overview at 6:45 PM; Presentation at 7:00 PM
Cost: none
Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara
RSVP: not required
Web: www.CaliforniaConsultants.org

Selling your services and being an effective consultant both require technologists to be clearly understood by non-technical business people. Insuring you are understood involves the following steps:

* Understand the business person's point of view,
* Learn the key words in the business person's vocabulary, and explain your services in those terms,
* Know which words in your own vocabulary are confusing or misleading to your audience, and
* Learn how to interpret the feedback you get

In this talk, John Levy will draw on his 20 years of consulting experience to describe what he has learned about how business people think - from Product Managers to Sales & Marketing Directors.

John Levy helps business managers who are frustrated because they are not getting what they need from their IT or Engineering organizations. He helps them get predictable, consistent and innovative results from high-tech people in IT and product development. John's clients include companies in insurance and manufacturing, as well as software, computers and storage.

John has held engineering management positions with Quantum Corporation, Apple Computer, Tandem Computers and Digital Equipment Corporation. He earned a Ph.D. in Computer Science from Stanford University, and holds engineering degrees from Cornell and Caltech. He is inventor or co-inventor on seven U.S. patents related to computer design.

John works as an expert witness in patent litigation related to computer, software and Internet technologies, and has been a technical advisor to two U.S. District Court judges. For two years, he co-produced West Marin Tech, a weekly radio show on technology and computers which was broadcast on KWMR in Point Reyes Station, CA. He is a regular teacher at the Fromm Institute of the University of San Francisco, with courses titled "The Digital Revolution in the Home and Computers - The Inside Story."

John's book on management for technology executives titled **Get Out of the Way** was published earlier this year.

SCV Computer, with ACM

TUESDAY September 14, 2010

Multicore Programming: Pitfalls and Solutions

Speaker: Madan Musuvathi, Researcher, Microsoft Research
Time: Networking with food and beverage at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation for food
Place: Microsoft Research (use rear/North door), 1288 Pear Ave., Mountain View
RSVP: required - from the website
Web: multicore.eventbrite.com

Madan Musuvathi is a researcher at Microsoft Research, where he focuses on concurrency analysis. He is interested in developing algorithms and tools that scale to and improve the reliability of large programs. Many of his tools are widely used by developers and testers inside Microsoft. He received his Ph.D. from Stanford University in 2004.

A big impediment in developing and maintaining concurrent software is our inability to effectively deal with race conditions. These "Heisenbugs" are hard to find. Even when found, they are hard to reproduce – making it next to impossible to debug and fix them. In this talk, Madan presents a series of tools from Microsoft Research that help developers and testers find, reproduce, and debug race conditions.

Madan will explain the theory underlying these tools and demonstrate their effectiveness in finding thread-safety violations, data races, deadlocks, and livelocks in product-quality software. The tools include CHESS, which uses model checking techniques to effectively unit test concurrent software, and Cuzz, which uses randomized algorithms to dramatically increase the bug-finding capability of existing concurrency tests. He will also explain various correctness criteria useful for developing reliable concurrent software.

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WEDNESDAY September 15, 2010

The Art of Catheter-Based Imaging

Speaker: Kendall R. Waters, PhD, Manager, IP and Technology Development, Silicon Valley Medical Instruments Inc.
Time: Optional dinner at Stanford Hospital Cafeteria, 6:15 PM (no host, no reservations); Presentation at 7:30 PM
Cost: none
Place: Room M-114, Stanford University Medical School, Stanford
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/embs

Dr. Kendall Waters is Manager of IP and Technology Development at the start-up Silicon Valley Medical Instruments, Inc. and an IEEE Senior Member. He is an expert in ultrasound, with particular experience in the interaction of ultrasound and tissue for diagnostic and therapeutic applications. He has previously worked at the Advanced Technology Laboratory of Volcano Corp, the National Institute of Standards and Technology and the Centre National de la Recherche Scientifique in France. Dr. Waters received his Ph.D. from Washington University in St. Louis, Missouri.

Catheters play a key role in diagnostic and therapeutic medicine. Nowhere is this more apparent than in the specialty of interventional cardiology, which is dedicated to catheter-based treatment of cardiovascular diseases. The tools of an interventional cardiologist include a variety of developed and emerging imaging technologies to guide therapy. This talk will focus not only on the science and engineering but also the on art of intracoronary imaging catheters. Intravascular ultrasound and optical coherence tomography catheter systems will serve as examples.

SCV Power Electronics

WEDNESDAY September 15, 2010

From Carbon-based to Sustainable Energy: What We Can Learn from "How Big Things Happen" in America

Speaker: Ray Rothrock, VENROCK
Time: Networking & Pizza at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/pels

Ray Rothrock joined Venrock in 1988 and after more than 20 years and over 40 investments, his passion for building companies continues. His venture capital career has its roots at Yankee Atomic Electric as a nuclear engineer, at Sun Microsystems and with two failed startups. An engineer at heart with a keen insight into product markets, Ray loves to tinker with technology. In addition to venture capital, he serves on the Board of Trustees of the Texas A&M Foundation, where he chairs the investment committee. Ray also serves on the Visiting Committee of the MIT Nuclear Science and Engineering Department and on the board of directors of NVCA.

Education:

B.S., Nuclear Engineering, Texas A&M University, summa cum laude
S.M., Nuclear Engineering, Massachusetts Institute of Technology
M.B.A., Harvard Business School, with Distinction

The United States is an amazing country, with a long history of innovation when it comes to solving big problems. With the freedom to publish, think, and argue, so many good things have come to pass for its citizens and the world – and probably some good things were missed, too. At Venrock this past year, we set out on a systematic journey through five decades of American business technology history to answer the question: where does innovation happen and when it does, how do big things happen in America? Our goal was apply what we learned to the most important challenge of our time: how to transition America from carbon-based to sustainable sources of energy.

Using simple pattern recognition of the many variables in business, academia, and innovation, we observed when and how America has achieved great things, and identified the key success factors that drove these achievements. Of course, there were failures, too, and understanding where and why these failings occurred was equally important to our task.

In this talk, Ray Rothrock, a Venrock partner and two-decade venture capitalist and energy investor, takes listeners through a brief history of the research and patterns that helped us determine how big things happen in America, and how what we learned can be applied to energy. The talk includes case studies. Then, with these learnings in hand, Ray applies them to the current situation in the United States, and world, regarding our energy future, what is at stake, and what needs to be done. Ray then presents an “If I were President” action plan of some controversy.

OEB Industry Applications

THURSDAY September 16, 2010

PV Solar Plants – Controls and Inverters

Speakers: Peter Kiggen, Manager, Emerson Control Techniques Solar Plant Solutions; Jim Cushman, Senior Account Manager, Emerson Process Management
Time: No-host social at 5:30 PM; Presentation at 6:15 PM; Dinner at 7:15 PM; Presentation continues at 8:00 PM
Cost: $20 for IEEE members; $25 for non-members
Place: Marie Callender's Restaurant - The Garden Room; 2090 Diamond Blvd, Concord
RSVP: by September 15, by contacting Gregg Boltz, gboltz@brwncald.com, (925) 210-2571
Web: www.e-grid.net/docs/1009-oeb-ias.pdf

Peter Kiggen is the Manager for Emerson Control Techniques Solar Plant Solutions, which manufactures Inverters for PV Plant Applications. **Jim Cushman** is Senior Account Manager for Emerson Process Management, Power and Water Solutions and is responsible for Plant Wide Controls in the Utility Scale Power Generation Market.

As the demand for Solar Power Generation increases through required regulation, there is a daily evolvement within the PV Solar Plant Development for Utility Scale Applications. Emerson will discuss how these plants are being developed by the Utilities and Financial Developers. This presentation will cover the following topics:

- Description of a Solar PV Plant
- Expectations from the Utilities
- How Inverters are utilized in a PV Solar Plant
- The need for Controls

SCV Control Systems

THURSDAY September 16, 2010

Patent Strategies for Entrepreneurs and Innovative Thinkers

Speaker: Dave Stevens, Stevens Law Group, P.C.
Time: Networking and refreshments at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Cogswell Polytechnical College, Board Room, 1175 Bordeaux Drive, Sunnyvale
RSVP: not required
Web: ewh.ieee.org/r6/scv/css

This presentation from a legal expert outlines general principles of intellectual property (IP) protection for various technologies, and will provide practical strategic planning tools and roadmaps for different types of companies and ventures. Case studies will provide working examples of IP roadmaps and strategies that have worked for successful startup ventures and fortune 500 companies. Ample time will be reserved for group questions, and also offline discussions afterwards.

Dave Stevens is a principal in the IP firm Stevens Law Group, PC. He has practiced IP law as a litigator, negotiator, and company builder for over 20 years. Dave specializes in startup company formation, and serves as legal counsel to numerous high tech startup companies. He is an industry expert on IP procurement and monetization, and lectures around the world on these and other global IP topics as they relate to various locales, technologies and legal fields.

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SCV Circuits and Systems

MONDAY September 20, 2010

Silicon Photonics: Opportunities & Challenges

Speaker: Dr. Haisheng Rong, Senior Scientist, Intel Labs
Time: Networking/light dinner at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation accepted for food
Place: QualComm Santa Clara, Building B, 3165 Kifer Road, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/cas

Silicon photonics technology offers promising low-cost optoelectronic solutions for many applications ranging from optical communications to emerging areas such as optical sensing and analysis. In recent years, rapid progress has been made in developing various silicon-based photonics building blocks. This talk will give an overview of research being done at Intel in the area of silicon photonics, highlighting the recent results and applications, and discussing the opportunities and challenges of optoelectronics integration.

Dr. Haisheng Rong is a senior scientist in the Photonics Technology Group of Intel Labs. He has worked in many areas of optical and laser technologies during his career including optical information processing, high-resolution laser spectroscopy, large-scale laser interferometer, and optical communications and interconnects. He has published numerous scientific papers including two in Nature and given over 20 invited and keynote presentations at major international conferences and meetings including SPIE conferences, CLEO, OFC, and LEOS meetings. He has won various Intel awards including the highest Intel Achievement Award. In November 2005, he was recognized by Scientific American as one of the top 50 research leaders in science and technology for his work on development of silicon Raman lasers. He received his Ph.D. degree from the University of Heidelberg, Germany. Prior to joining Intel Corporation, he also held engineering position at New Focus, and research positions at MIT and Caltech. He is a Senior Member of IEEE.

SCV Nanotechnology

TUESDAY September 21, 2010

SolFocus Concentrator Photovoltaics – An Introduction

Speaker: Dr. Phil Metz, Director of Business Development, SolFocus
Time: Registration & light lunch 11:30 AM; Presentation at 12:00 Noon
Cost: IEEE Members and Students $5; Non-Members $10
Place: National Semiconductor Bldg E-1 CMA Room. 2900 Semiconductor Drive, Santa Clara
RSVP: from the website
Web: www.ieee.org/nano

Dr. Phil Metz leads Business Development with energy developers in North America for SolFocus, a leader in the Concentrator Photovoltaic (CPV) industry. In this role Dr. Metz builds strategic partnerships and drives sales with selected developers in key vertical markets and geographies.

Prior to joining SolFocus he was Vice President, Market Planning and Sales Support, and subsequently Vice President Self-Service Automation, at Solectron, a $12B+ electronics manufacturing services leader. Dr. Metz' background includes 12 years of management consulting in energy, strategy, marketing and technology management, 10 years of renewable energy R&D, and a PhD in physics.

This presentation introduces the SolFocus Concentrator Photovoltaic (CPV) product – what it is and how it works. It presents the value proposition for SolFocus CPV and the design and manufacturing advantages of this product vs. other solar options, supplemented by a discussion of where to use SolFocus CPV and examples and data from existing installations.

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SCV Magnetics

TUESDAY September 21, 2010

Thermally-Assisted Magnetic Recording at up to 1 Tb/in^2 using an Integrated Plasmonic Antenna

Speaker: Barry Stipe, Hitachi Global Storage Technologies
Time: Networking and pizza at 7:00 PM; Presentation at 7:30 PM
Cost: none
Place: Western Digital, 1710 Automation Parkway, San Jose
RSVP: not required
Web: ewh.ieee.org/r6/scv/mag

Barry Stipe received a B.S. in physics from Caltech in 1991 and a Ph.D. in physics from Cornell University in 1998. His thesis research at Cornell included the first demonstrations of single molecule vibrational spectroscopy and manipulation using a scanning tunneling microscope, for which he won the Morton M. Traum Award and Nottingham Prize. For his postdoc at the IBM Almaden Research Center, Barry worked toward the imaging of single spins using magnetic resonance force microscopy which was later achieved by the IBM team. Since 2000, Barry has worked on data storage technology for IBM and now Hitachi-GST as a research staff member. Barry's work at HGST has included concepts for ultra-low head-disk spacing, improved drive mechanics for reducing track pitch, new materials for perpendicular media, solid-state memory, plasmonics, head integration, and read-write testing.

Barry is leading HGST's efforts to circumvent the scaling limits of conventional hard drive technology through the development of thermally assisted magnetic recording. Barry has written a number of highly cited works including five papers with more than 100 citations each. He has filed more than 30 US patents.

Thermally-Assisted Magnetic Recording (TAR) and Bit Patterned Recording (BPR) are two of the most promising technologies for surpassing the fundamental limitations of conventional magnetic recording. In a typical TAR head design, a waveguide delivers light to a plasmonic aperture or antenna located at the air-bearing surface. The plasmonic device creates an intense optical pattern in the near-field, heating the disk at the nanometer scale. This writing technique allows one to use extremely high anisotropy media (such as L10 FePt) for reduced grain size while maintaining the requirements of thermal stability and writability. We have fully integrated a plasmonic antenna called the "E-antenna" into a magnetic head and then used it for recording on granular media with a static tester and spin stand.

So far, TAR at over 400 Gb/in^2 has been limited by the availability of a suitable small grain media. BPR avoids the need for small grain media but it can be difficult to address the patterned bits at very small track pitch using a conventional write head. We have recently found that combining TAR and bit-patterned media (BP-TAR) can solve both problems and allows for dramatic reductions in track pitch (down to 24 nm) and optical power requirements (factor of five) as compared to TAR recording on granular media. We show recording at up to 1 Tb/in^2. BP-TAR may turn out to be the ultimate HDD technology and is, in principle, scalable to 100 Tb/in^2.

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THURSDAY September 23, 2010

Design of High Density & 3D Packaging: Tools and Knowledge

Speaker: Thomas Tarter, Package Science Services LLC
Time: Registration & social at 11:30 AM; Optional lunch at 11:45 AM; Presentation at 12:15 PM
Cost: $15 for lunch; Students & unemployed members $5 (no cost for presentation-only)
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: From the website
Web: www.cpmt.org/scv

Thomas S. Tarter is an expert on thermal management, thermal and electrical characterization, and design of microelectronic and optoelectronic packaging structures. He spent 17 years at AMD in package characterization and was a Senior Member of the Technical Staff. Subsequently he was Director of BGA Package Engineering and Design at Advanced Interconnect Technology, and Principal Engineer for thermal management, temperature control and package development at NeoPhotonics Corporation, Inc. In 2009, Tom started Package Science Services LLC, to serve the high-tech community with electronic packaging expertise in design, analysis, and characterization (electrical, thermal, reliability) and support all phases of IC, solar cell, LED and other chip packaging from concept to hand off to mass manufacturing.

Tom has published 30 papers, holds 5 patents, and has presented numerous short courses and lectures. He chaired the JEDEC JC15.1 task group on thermal standards for five years, was general chair of SEMI-THERM, Technical Chair for five years, and serves on the SEMI-THERM executive committee to date. Tom is a senior member of IEEE and was chair of the IEEE Santa Clara Valley Chapter of CPMT for two years. Society affiliations include, IEEE, LEOS, Santa Clara Valley Nanotechnology Council, MEPTEC, IMAPS, and SPIE.

Packaging of complex silicon devices requires a deep knowledge of many aspects of high-technology engineering disciplines. As an example, packaging a high lead-count chip requires knowledge of electrical, thermal, mechanical, chemical and manufacturing engineering. These disciplines must be known and must be used in the conceptualization, design and implementation of any package design. Complex systems many times require more than one die in the package. These chips can be stacked or arrayed onto a substrate to increase functionality and reduce size and cost, driving the complexity of the package beyond the capability of simple drawings and 2D design tools. 3D packaging creates challenges in the characterization and validation of thermal, electrical and mechanical functionality.

This presentation provides an overview of package design for high-density, 3D products with a focus on the electrical characterization challenges. The talk will cover approaches for parameter extraction, high-frequency modeling and simulation and the need for advances and features in 3D design programs, and will go over a typical design flow for high-performance package development and implementation.

SCV Communications, with NATEA

SATURDAY September 25, 2010

Smart Grid Workshop: M2M Communications, Emerging Devices and "The Internet of Things"

Speakers: Claudio Lima, IEEE P2030 Smart Grid Architecture Standards WG; Stefano Galli, Panasonic R&D; Kuor-Hsin Chang, Elster Solutions; Jeffrey Smith, Numerex Corp, Jason Porter, AT&T; Michael Finegan, Sprint Emerging Solutions Group
Time: Presentations from 1:00 PM - 7:00 PM in two tracks
Cost: IEEE Members, students, unemployed $10; non-members $20
Place: Benson Center, Santa Clara University, Santa Clara
RSVP: From the website
Web: www.ewh.ieee.org/r6/scv/comsoc

Program

Track I: **Communications Aspects of Smart Grids**

- **Smart Grid Communications: Enabling a Smarter Grid**, Claudio Lima, Vice Chair of IEEE P2030 Smart Grid Architecture Standards WG
- **Power Line Communications and the Smart Grid,** Stefano Galli, Lead Scientist Panasonic R&D
- **Wireless Communications for Smart Grid,** Kuor-Hsin Chang, Principal System Engineer - Standards, Elster Solutions

Track II: **Smart Devices, and Network Aspects of M2M Communications**

- **Standardization as a Catalyst of M2M Market Expansion,** Jeffrey Smith, Chief Technology Officer, Numerex Corp
- **Operations and Management of Mobility Applications and M2M Networks**, Jason Porter, AT&T
- **Sprint's Machine-to-Machine and Service Enablement Platform**, Michael Finegan, West Area M2M Manager of Solutions Engineering, Sprint Emerging Solutions Group

TUESDAY September 28, 2010

Short Circuit, Device Coordination, and Arc Flash Analysis

Speaker: Alberto Marroquin, P.E., Operation Technology, Inc
Time: Social at 5:30 PM; Presentation at 6:00 PM; Dinner at 7:00 PM
Cost: $30 (at the door); $10 for student members. Email pre-registration qualifies the registrant for our drawing of an IEEE Color Book at dinner.
Place: Sinbad's Restaurant, Pier 2 The Embarcadero, San Francisco
RSVP: by email, to Frank Sylvester, SFPUC, fsylvester@sfwater.org, 415-554-1578
Web: ewh.ieee.org/r6/san_francisco/ias

Alberto Marroquin is an active contributor to IEEE 1584 and NFPA 70E committees and a member of IEEE P181/D1 (Draft Recommended Practice for Electrical System Design Techniques to Improve Electrical Safety). He joined Operation Technology, Inc in January 2001 as an Electrical Engineer. His current position with OTI is Principal Electrical Engineer.

This presentation will introduce some on the latest trends in short-circuit and device coordination and their relationship to arc flash analysis. The presentation will also cover some new concepts which are in development and may become part of future editions of the existing guidelines like IEEE 1584 and NFPA 70E. The protection schemes to be discussed include Zone Selective Interlocking and Selective Instantaneous Protection and their impact in the reduction of the incident energy exposure including simulation results for typical applications. The presentation will also cover the latest trends in arc flash analysis from IEEE 1584 and NFPA 70E 2009 including systems not covered by any guidelines like low voltage systems fed by small transformers (less than 125 kVA @ 208 VAC) and direct current arc flash calculations which may be added to the next edition of NFPA 70E 2011. The presentation will also touch on some relatively unknown special arc flash calculations for generation plants with transient short-circuit fault current contribution and special excitation protection including differential and field current discharge.

SCV Product Safety Engineering

TUESDAY September 28, 2010

What's in Your Electronic Product, and Why Should a Product Safety Engineer be Concerned?

Speaker: Rick Row, Consultant
Time: Optional dinner at 5:30 PM; Presentation at 6:30 PM
Cost: no-host dinner at El Torito Mexican Restaurant; no cost for presentation
Place: Dinner at El Torito Mexican Restaurant, 2950 Lakeside Drive, Santa Clara; Meeting at Applied Materials, Bowers Café, 3090 Bowers Ave, Santa Clara
RSVP: not required
Web: ewh.ieee.org/r6/scv/pses

Rick Row is currently consulting on energy efficiency and low-carbon energy generation and use, and on compliance with environmental regulations. From 2007 to 2009, he was the Executive Director of Sustainable Silicon Valley, a non-profit that partners with businesses, governments, and other non-profit organizations in Silicon Valley to create a more sustainable future. Partners pledge to SSV to set their own CO_2 reduction targets, report annually to SSV on their performance against their targets, and collaborate with SSV to share their CO_2 reduction success stories publicly.

For the previous five years, he managed Global Care, an environmental, health and safety (EHS) initiative, in the EHS Division at SEMI, a global industry association for companies providing equipment, materials and services used to manufacture semiconductors and related technologies. He also worked with EHS professionals in the industry to guide the industry's response to environmental regulations such as the European Union's WEEE and RoHS directives, and China's "China RoHS".

Three trends make mineral sourcing an issue of potentially compelling interest to product safety engineers. First, many more minerals are used today in manufacturing electronics than just a couple of decades ago. For example, Intel estimates that, whereas computer chips contained 11 mineral-derived elements in the 1980s, potentially up to 60 elements will be used in coming years. Second, the downstream manufacturer is being held increasingly accountable for the traceability and regulation of materials in his product. Such traceability has commonly been non-existent for many complex electronic products. Section 1502 of the Dodd-Frank Wall St. Reform and Consumer Protection Act, signed into law on July 21, 2010, will require U.S. public companies to disclosure the use of "conflict minerals," such as tantalum from the Democratic Republic of the Congo, in manufacturing their products; and over 60 percent of tantalum used in the U.S. is used in capacitors. This law imposes a social responsibility on manufacturers, and adds to a growing international pattern of laws and regulations with environmental and public health and safety objectives. Finally, concern is growing in some quarters about the availability, pricing, and sourcing of minerals (some of which are difficult to replace in certain electronic applications) as global demand rises, the grade of mineral deposits decline over time, and competitors such as China threaten to "lock-up" supplies of rare earth minerals. Because earlier material concerns have risen through the need to comply with EHS regulations such as the RoHS, WEEE, and REACH directives in the European Union, product safety engineers are as well-placed as any professionals in the electronics industry to take on a key company-wide coordinating role to help their companies and industry remain profitable and resilient in the face of these trends.

WEDNESDAY September 29, 2010

Development and Application of Accelerated Test Methods Specific to CPV Systems

Speaker: Mark Spencer, Staff Reliability Engineer, SolFocus
Time: Social/refreshments at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Hewlett Packard Oak Room, Bldg 48, 1911 Pruneridge Ave, Cupertino
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/rl

Mark Spencer received a BS degree in Environmental Resources Engineering from Humboldt State University and a MS degree in Mechanical Engineering from the University of Hawaii. He has worked for 15 years in the power generation industry. During the first 10 years he worked on low-NOx combustion systems for advanced industrial gas turbines. Switching to solar power, he has worked at SolFocus for nearly 5 years, working on concentrator photovoltaic design, quality and reliability.

SolFocus is currently involved in two separate accelerated test efforts to quantify the long term life of its SF1100 CPV (concentrator photovoltaic) product. Results from these tests will be correlated with the ongoing monitoring of non-accelerated systems operating in the field, and the resulting relationships used to predict lifetime. This paper details the accelerated test methodology used, presents some preliminary test results and links those results to standard operating conditions.

See also the Rel Chapter talk on October 27th, "**HCPV Tracker Accelerated Reliability Tests**" (later in this GRID issue), for a continuation of this topic.

OEB Life Members

TUESDAY October 5, 2010

Kickoff Meeting - IEEE Life Members Affinity Group

Speaker/organizer: Charles Herget, Lawrence Livermore National Laboratory (retired)
Time: Networking, buffet dinner, discussion from 6:00 PM - 8:00 PM
Cost: $10 for buffet dinner
Place: Willow Tree Restaurant, 6513 Regional St, Dublin
RSVP: by October 1, through website
Web: www.ieee4life.org

Charles Herget was recorded as chair of the Affinity Group by IEEE after collecting the required signatures to petition IEEE to form this group. He is retired from Lawrence Livermore National Laboratory. He has been active in IEEE for over 40 years. He has served as President of the IEEE Control Systems Society, the IEEE Council on Intelligent Transportation Systems, and the IEEE Intelligent Transportation Systems Society.

The first meeting of the Oakland/East Bay Life Member's Affinity Group will be held on Tuesday, October 5, 2010, at the Willow Tree Restaurant in Dublin. This meeting will be an informal gathering to discuss our organization, topics of interest, frequency, and location of meetings. The meeting is open to anyone interested in participating, not just IEEE Life Members. We expect the topics that will be the subject of future meetings will be as diverse as the Life Members themselves, covering subjects such as energy, environment, education, as well as retirement activities. We anticipate lively discussions at our upcoming meetings. Please come and get acquainted.

SCV Technology Management

THURSDAY October 7, 2010

Building Powerful Relationships

Speaker: Jay Orlin, Learning and Development Leader
Time: Networking at 6:00 PM; Forum at 6:30 PM; Dinner at 7:15 PM; Presentation at 7:45 PM
Cost: $10 for IEEE members; $13 for others
Place: RAMADA Silicon Valley, 1217 Wildwood Ave, Sunnyvale
RSVP: not required
Web: www.ieee-scv-tmc.org/

Jay Orlin is a long-time Silicon Valley Learning and Development thought leader. He has managed training for Intel, Nortel, Tandem, Altera and Philips Medical Systems. He has also consulted to many other companies such as Hewlett Packard, Cisco, Bayer Pharmaceuticals, Raychem, Avery Dennison, Pac Bell and Sun Microsystems.

Goal:

Participants will establish increased trust and rapport with co-workers by approaching communication with an understanding of diverse personalities, backgrounds and communication preferences

Performance Objectives:

- Gain awareness of Temperament Types
- Understand how Temperaments influence relationships
- Improve ability to handle people who are upset

Description:

In a lively 45- minute session you will learn how to interpret your own and other people's behaviors in ways that promote better understanding and communication possibilities. You will also gain practical techniques to de-escalate conflict situations. Participants will receive handouts that will be valuable in implementing what they learn.

SCV Computer

TUESDAY October 12, 2010

High Performance Computing: Union of Software and Reconfigurable Logic

Speaker: Ivo Bolsens, Senior VP and CTO, Xilinx
Time: Networking with food and beverage at 6:30 PM;
Presentation at 7:00 PM
Cost: $2 donation for food
Place: Microsoft Research (use rear/North door),
1288 Pear Ave., Mountain View
RSVP: required - from the website
Web: fastcomputing.eventbrite.com

Ivo Bolsens is senior vice president and chief technology officer (CTO) of Xilinx, with responsibility for advanced technology development, Xilinx research laboratories and Xilinx university program. Bolsens came to Xilinx in 2001 from the Belgium-based IMEC, where he was vice president of System Design R&D. His responsibilities included the HW and SW development of ASSP's for of digital signal processing applications and wireless communication terminals. He also headed the activities on tool development for HW/SW co-design and system-on-chip design.

Bolsens holds a PhD and an MSEE from the Catholic University of Leuven in Belgium.

Modern FPGA platforms have capabilities that are well suited to assume a more central role in the implementation of complex embedded processing systems. In particular, FPGAs are well placed to be at the heart of complex signal processing, packet processing and high performance computing applications because of their high computational efficiency matched by high-bandwidth concurrent memory access and rich on-chip interconnectivity, all of this combined with complete programmability.

The key to unleashing the full horsepower of FPGA platforms to the system designer is, first of all, a hardware platform that allows tight integration between the processor, the programmable logic and the memory. Second, the hardware architecture has to be supported by a programming flow that abstracts the hardware implementation details and provides seamless and efficient mapping of system functions on multiple processor cores and programmable hardware functions. Finally, a programmable infrastructure has to be provided that targets specific requirements for packet processing, signal processing, or high performance computing.

TUESDAY October 12, 2010

All-Silicon System with Nano-Packaging: Highest Functionality, Lowest Cost, Smallest Size

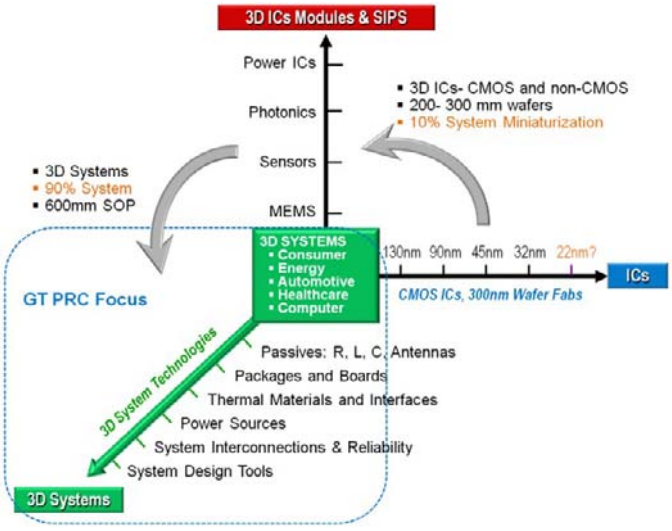
Speaker: Prof. Rao Tummala, Founding Director, NSF Packaging Research Center, Georgia Tech
Time: Optional dinner at 6:00 PM; Presentation at 6:45 PM
Cost: $20 for dinner; Students & unemployed members $10 (no cost for presentation-only)
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: From the website
Web: www.cpmt.org/scv

Prof. Rao Tummala is a Distinguished and Endowed Chair Professor, and Founding Director of NSF PRC at Georgia Tech, the largest Academic Center in Microsystems pioneering the System-On-Package (SOP) vision, since 1994. Prior to joining Georgia Tech, he was an IBM Fellow, pioneering such major technologies as the first plasma flat panel display based on gas discharge, the first and next three generations of multichip packaging based on 35-layer alumina and 61-layer LTCC with copper and copper-polymer thin film, and materials for ink-jet printing and magnetic storage.

He has received many industry, academic and professional society awards including Industry Week's award for improving U.S. competitiveness, IEEE's David Sarnoff, Major Education and Sustained Technical Contribution awards, Engineering Materials Achievement award from DVM and ASM-International, Total Excellence in Manufacturing award from SME, and the John Jeppson's award from the American Ceramic Society. He received his BS from IISc, Bangalore and his Ph.D. from the University of Illinois.

Prof. Tummala has published 426 technical papers, holds 74 patents and inventions; authored the first modern packaging reference book **Microelectronics Packaging Handbook** (Van Nostrand, 1988), the first undergrad textbook **Fundamentals of Microsystems Packaging** (McGraw Hill, 2001) and the first book introducing System-On-Package technology. He is a Fellow of the IEEE, IMAPS, and the American Ceramic Society, and member of the National Academy of Engineering in the USA and in India. He has served as President of both the IEEE-CPMT Society and IMAPS.

Nanopackaging has been defined as the process of interconnecting, powering, cooling, and protecting the nanocomponents made of nanomaterials to form electronic and bioelectronic systems for greatly improved functionality and cost. In spite of Si CMOS-based active devices at 32 nm with a billion transistors, today's systems are limited by bulky, milliscale components that make up 90% of the system. In addition, the future of Si CMOS beyond 22 nm seems uncertain and the industry has shifted its R&D investments to three-dimensional (3D) ICs with through-silicon vias (TSVs). But 2D and 3-D ICs are a small part of any system, and the functionality per unit volume of the system can only be improved dramatically by miniaturization of non-active system components as shown in the illustration.



The X axis represents the progress in Si CMOS-based devices; the Y axis represents the expected progress in 3-D ICs, not only in CMOS but also in heterogeneous ICs; and the Z axis represents Georgia Tech's 3D nanopackaging approach to miniaturize the entire system. The focus of the Z axis for the entire system is with nanoscale passives, thermal interfaces, batteries, and interconnections, all of which are being integrated into highly miniaturized systems leading to unparalleled miniaturization, functionality, and cost. Such an approach with nanoscale-active devices and nanoscale system components can lead to an all-silicon systems platform.

This presentation focuses on a variety of nanoscale materials, processes, and components to enable such a vision.

Consider attending Rao Tummala's afternoon Seminar, from 3:30 - 5:30 PM (see website), then staying for dinner and this evening talk.

SCV Electron Devices

TUESDAY October 12, 2010

Is It the End of the Road for Silicon in Power Management?

Speaker: Dr. Alex Lidow, CEO, Efficient Power Conversion
Time: Networking with pizza at 6:00 PM; Presentation at 6:15 PM
Cost: none
Place: National Semiconductor, Building E-1, Conference Center, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds

Alex Lidow is Co-founder and CEO of Efficient Power Conversion Corporation (EPC). EPC designs, develops, and produces Gallium-Nitride-on-Silicon transistors and integrated circuits used in power management. Prior to founding EPC, Dr. Lidow was chief executive officer of International Rectifier Corporation, a company he joined in 1977. A co-inventor of the HEXFET power MOSFET, Dr. Lidow holds many patents in power semiconductor technology and has authored numerous publications on related subjects. Alex earned his BS in applied physics from Caltech in 1975 and his PhD in applied physics from Stanford in 1977 as a Hertz Foundation Fellow.

For the past three decades, power management efficiency and cost have shown steady improvement as innovations in power MOSFET structures, technology, and circuit topologies have paced the growing need for electrical power in our daily lives. In the last few years, however, the rate of improvement has slowed as the silicon power MOSFET has asymptotically approached its theoretical bounds. We will address the new game-changing power management products, available today and planned for the near future, that are built on Gallium Nitride grown on top of a silicon substrate. Enhancement mode devices, first introduced in June 2009, will be demonstrated in DC-DC conversion and Class D audio applications. GaN roadmaps for improved device performance and for system-on-chip integration will also be discussed. Performance is only one dimension on the equation leading to the conclusion that GaN-on-silicon is a game-changer. The other dimensions are product reliability and cost. These topics will also be discussed showing that the capability to displace silicon across a significant portion of the power management market is now in hand.

WEDNESDAY October 13, 2010

40/100 Gigabit Ethernet: Market Needs, Applications, and Standards

Speakers: John D'Ambrosia, Force10 Networks; Ilango Ganga, LAN Access Division, Intel
Time: Networking with Cheese, Crackers, Drinks at 6:00 PM; Presentations at 6:30 PM
Cost: none
Place: National Semiconductor, Building E, Conference Room, 2900 Semiconductor Dr, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/comsoc

John D'Ambrosia leads Force10 Networks' involvement in industry groups. John has been an active participant in the development of Ethernet-related technologies since 1999. Recently, John served as the chair of the IEEE P802.3ba Task Force, which developed 40 Gb/s and 100 Gb/s Ethernet. Prior, John served as secretary for the IEEE 802.3ap Backplane Ethernet Task Force, and participated in the development of XAUI for 10 Gigabit Ethernet. John is a founder of the Ethernet Alliance and has served as a director and secretary. John was the chair of the XAUI Interoperability work group for the 10 Gigabit Ethernet Alliance. For all of his efforts related to Ethernet, John was recognized by Network World in 2006 as part of its "50 Most Powerful People in Networking" list. John also acted as secretary for the High Speed Backplane Initiative and chair of the Optical Internetworking Forum's Market Awareness & Education committee. Prior to joining Force10, John was with Tyco Electronics for 17 years.

Ilango Ganga is a Server Communications Architect at Intel's LAN Access Division. Ilango is responsible for architecting next generation Ethernet technologies including higher speed Ethernet, I/O virtualization and data center communications for LAN controller products. Ilango has over 19 years of industry experience in the area of Ethernet communications, blade server networking, switch silicon development and has held various roles in hardware design, engineering management, architecture, and product planning. Ilango is an active contributor to the Ethernet standards development including backplane Ethernet, data center bridging and edge virtual bridging. He recently served as the Chief Editor of the IEEE P802.3ba 40Gb/s and 100Gb/s Ethernet task force. Ilango has 7 patents pending in the area of networking technology.

Ethernet's Next Evolution – 40GbE and 100GbE

This talk will provide an overview of the Ethernet Eco-system and the applications within that drove the need for the development of IEEE Std. 802.3baTM-2010 40Gb/s and 100Gb/s Ethernet Standard. Technology trends in computing and network aggregation and their role in driving the market need for 40GbE and 100GbE will be discussed.

The IEEE Std 802.3ba-2010 40Gb/s and 100Gb/s Architecture

This talk provides an overview of IEEE Std 802.3ba-2010 40Gb/s and 100Gb/s Ethernet specifications, objectives, architecture and interfaces.

The next generation higher speed Ethernet addresses the needs of computing, aggregation and core networking applications with dual data rates of 40Gb/s and 100 Gb/s. The 40/100 Gigabit Ethernet (GbE) architecture allows flexibility, scalability and leverages existing 10 Gigabit standards and technology where possible. The IEEE Std 802.3ba-2010 provides physical layer specifications for Ethernet communication across copper backplane, copper cabling, single-mode and multi-mode optical cabling systems.

The 40/100 Gigabit Ethernet utilizes the IEEE 802.3 Media Access Control sublayer (MAC) coupled to a family of 40 and 100 Gigabit physical layer devices (PHY). The layered architecture includes multilane physical coding sublayer (PCS), physical medium attachment sublayer (PMA) and physical medium dependant sublayers (PMD) for interfacing to various physical media. It also includes an Auto-Negotiation sublayer (AN) and an optional forward error correction sublayer (FEC) for backplane and copper cabling PHYs. The optional management data input/output interface (MDIO) is used for connection between 40/100 GbE physical layer devices and station management entities. The architecture includes optional 40 and 100 Gigabit Media Independent Interfaces to provide a logical interconnection between the MAC and the Physical Layer entities. It includes 40 and 100 Gigabit attachment unit interfaces (XLAUI and CAUI), four or ten lane interface, intended for use in chip-to-chip or chip-to-module applications. It also includes a 40 and 100 Gigabit parallel physical interface, four or ten lane non-retimed interface, intended for use in chip-to-module applications with certain optical PHYs. The presentation will also outline the applications for some of the above interfaces.

SCV Circuits and Systems

MONDAY October 18, 2010

Automated Behavioral Modeling: A Quantum Jump in Mixed-Signal Design Verification Technologies

Speaker: Prof. Richard Shi, University of Washington
Time: Networking/light dinner at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation accepted for food
Place: QualComm Santa Clara, Building B, 3165 Kifer Road, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/cas

Verification is becoming the number-one bottleneck in mixed-signal systems-on-chip (SoC) design. This talk introduces a new design and verification methodology based on the automated generation of high-level behavioral models from a SPICE netlist. The new methodology is fully compatible with existing design flows yet offers 100x to 1000x reduction in the SPICE simulation time. Analog assertions can be automated, paralleling the well-accepted digital verification methodology.

Richard Shi is a Professor in Electrical Engineering at the University of Washington, Seattle, where he is teaching VLSI design. He has supervised over 20 PhD students and post-doctoral fellows in the area of circuit simulation, model compilation, analog layout automation, cirucit optimization, and behavioral modeling. He has served as an Associate Editor for IEEE Transactions on Computer-Aided Design for the past ten years. He received several best paper awards including Donald Pederson Best Paper Award. He advised two EDA startups Apteq (A Verilog-A compiler Company) and Gemini (A Parallel SPICE company): both acquired by Synopsys. He is a co-founder of Orora Design Technologies, Inc., focusing on automating mixed-signal design and verification. He has been elected to an Fellow of IEEE for his contribution on computer-aided design of mixed-signal integrated circuits.

SCV Solid State Circuits, with Signal Processing, Circuits and Systems, and Communications

THURSDAY October 21, 2010

Tutorial: Status of Knowledge on Non-Binary LDPC Decoders

Speaker: Prof. David Declercq, ENSEA in Cergy-Pontoise
Time: Networking and snacks at 5:30 PM; Lecture at 6:00 PM
Cost: $2 donation accepted for food
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Dr., Santa Clara
RSVP: from website
Web: ewh.ieee.org/mu/scv-sscs

David Declercq graduated with his PhD in Statistical Signal Processing 1998. He worked on a new Gaussianity test based on Hermite polynomials properties, and the characterization and the blind identification of non-linear time series. After his PhD, he oriented his research towards digital communications, and especially coding theory and iterative decoder design. He started to work on LDPC codes in 1999, both from the code and decoder design aspects.

Since 2003, he has made a major effort in studying and developping LDPC codes and decoders in high order Galois fields GF(q), with q>>2. A large part of his research projects are related to non binary LDPC codes. He mainly investigated two directions: (i) the design of GF(q) LDPC codes for short and moderate lengths, and (ii) the simplification of the iterative decoders for GF(q) LDPC codes with complexity/ performance tradeoff constraints.

David Declercq has published more than 20 papers in major journals (IEEE-Trans. Commun., IEEE-Trans. Inf. Theo., Commun. Letters, EURASIP JWCN), and more than 70 papers in major conferences in ICT. He is currently a full professor at the ENSEA in Cergy-Pontoise, France, a graduate school in Electrical Engineering. He is a member of the ETIS laboratory, general secretary of the National GRETSI association, and member of the GdR-ISIS direction team. He is currently the recipient of a junior position at the “Institut Universitaire de France”.

In this tutorial, the iterative decoding techniques for non-binary LDPC codes will be presented, both from the theoretical aspects of Belief Propagation and its analysis, and from more practical aspects of efficient implementation. In a first part, the main difference between iterative BP decoding of binary and non-binary LDPC codes will be highlighted. Then, in a second part, the solutions proposed in the literature to reduce the complexity of non-binary decoders, both for memory storage and computational burden reduction, will be presented. Some directions of research and development about non-binary decoders will be discussed. Finally, the outstanding advantages of generalized non-binary decoders on clustered graphical models of several error correcting codes will be presented.

WEDNESDAY October 27, 2010

HCPV Tracker Accelerated Reliability Tests

Speaker: Jon G. Elerath, Staff Reliability Engineer, SolFocus
Time: Social/refreshments at 6:30 PM; Presentation at 7:00 PM
Cost: none
Place: Hewlett Packard Oak Room, Bldg 48, 1911 Pruneridge Ave, Cupertino
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/rl

Jon Elerath received the BSME and MS Reliability degrees from the University of Arizona and the PhD degree in mechanical engineering from the University of Maryland. He has been a reliability engineer or reliability manager at the General Electric Co., Tegal, Tandem Computers, Compaq, IBM, and NetApp . He is currently a Staff Reliability Engineer at SolFocus. He has applied reliability techniques to nuclear safety systems of fast breeder reactors, electronics and robotics of plasma-etching equipment, fault-tolerant computers, hard disk drive designs, RAID data storage systems, and concentrated photovoltaic mechanical tracking systems. He has authored more than 30 technical publications on reliability. Currently, his major area of interest is hardware reliability of solar trackers. He is active in writing IEEE reliability standards, including IEEE 1413 and the guide, IEEE 1413.1. He is a member of the IEEE.

An accelerated reliability test plan was developed for trackers used in high-concentration photo-voltaic power systems. The potential failure modes of the tracker hardware were used to select the hardware that was tested. The 2-parameter Weibull distribution was used as the underlying time-to-failure distribution. Equations used to help identify degrading bearings and gears were based on vibration frequency analysis. Results show that the accelerated life test identified wear-in as well as wear-out mechanisms.

THURSDAY October 28, 2010

Good Things Come in Small Packages

Speaker: Sandra Winkler, New Venture Research
Time: Registration & social at 11:30 AM; Optional lunch at 11:45 AM; Presentation at 12:15 PM
Cost: $15 for lunch; Students & unemployed members $5 (no cost for presentation-only)
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: From the website
Web: www.cpmt.org/scv

Sandra Winkler has been an industry analyst since 1988, as an independent consultant, as a staff member of Electronic Trend Publications, and currently for New Venture Research. She has produced numerous off-the-shelf and custom reports. Ms. Winkler began her analyst career in the telecommunications industry. Since 1995, she has focused on the semiconductor packaging industry, and has authored a number of widely cited reports on the topic, including The Worldwide IC Packaging Market, Advanced IC Packaging Markets and Trends, and IC Packaging Materials. She also writes for Chip Scale Review Magazine. Ms. Winkler has an MBA from Santa Clara University. She is on the executive planning committee of the IEEE-CPMT Santa Clara Valley chapter.

The semiconductor industry has experienced strong growth in 2010, despite a weak and uncertain economy. Inexpensive ($300-400 and under) consumer electronics products are the driving force of semiconductor sales. Particularly doing well are devices and packages suited for handheld units that offer consumers portable connectivity and high performance, at a low cost. The growth trends of QFN, WLP and stacked packages, as well as TSVs (through-silicon-vias) will be the focus of this review, as well as the global outlook of the overall economy and the IC packaging market in general.

WEDNESDAY November 10, 2010

Embedded Passives: Packaging Paradigm of the Future?

Speaker: Jason Ferguson, Crane Naval Surface Warfare Center
Time: Optional dinner at 6:00 PM; Presentation at 6:45 PM
Cost: IEEE members $40; Non-members $50; Students & unemployed members $20 (Optional box lunch add $10)
Place: Engineering Building Auditorium, ENG 189, San Jose State University, One Washington Square, San Jose
RSVP: required - from the website
Web: www.cpmt.org/scv

Embedded Passive (EP) Technology is of interest to many OEMs and designers, but the technology remains a mystery for how and when to implement this technology into designs.

Embedded passives will be the next pivotal technology for PCBs. Simply stated, embedded passives are the incorporation (embedding or burying) of passive components, particularly resistors and capacitors, in a substrate. Around in some form for years, EPs are now seen as a key enabling technology in the National Electronics Manufacturing Initiative (iNEMI) Roadmap. The EP revolution is soon to come."

This presentation will reveal what EP materials are out on the market, what the benefits are for using the technology, and give examples of when implementation is viable to a design.

Jason Ferguson holds a Bachelor of Science degree from Rose-Hulman Institute of Technology. In 1995, he began a four year tour of duty as a commissioned officer in the U.S. Army. After his service, he went to work for the Naval Surface Warfare Center at Crane, IN. For the past ten years, he has served as a systems engineer on an air defense program called Cooperative Engagement Capability and as a process engineer for the printed circuit board (PCB) fabrication shop. For the past six years, he has been fabricating and testing embedded passive technology in PCB's. This has led to a project with the Jet Propulsion Lab at Cal Tech to embed resistors and capacitors into a current motor controller design to demonstrate electrical and reliability performance.